Claims

We claim:

1. A semiconductor die containing an MIS device, said die comprising a first layer of a first conductivity type overlying a second layer of a second conductivity type opposite to said first conductivity type, said die further comprising:

an active area comprising an MIS device, said MIS device comprising:

an active trench comprising a conductive gate material and extending downward from a surface of said first layer, a bottom of said active trench being located in said first layer;

a source region of said second conductivity type in said first layer, said source region being located adjacent said surface of said die and a sidewall of said active trench; and

a drain-drift region of said second conductivity type extending downward from said bottom of said active trench to said second layer; and

a termination region comprising:

at least a first and a second termination trench, each of said termination trenches extending downward from said surface of said die, each of said termination trenches comprising a conductive material and having a bottom in said first layer, said conductive material in each of said termination trenches being insulated from said first layer by a dielectric layer lining the sidewalls and bottom of said termination trench;

a region of said second conductivity type extending from a bottom of each of said termination trenches to said first layer;

at least a first and a second metal layer above said surface of said die, said first metal layer being electrically connected to said conductive material in said first termination trench and to a portion of said second layer in a mesa between said first and second trenches, said second metal layer being electrically connected to said conductive material in said second termination trench and to a portion of said second layer in a region on a side of said second termination trench opposite from said mesa, wherein said conductive materials

in said termination trenches are electrically isolated from each other and from said source region and said first layer.

2. The semiconductor die of Claim 1 wherein the conductive material in the first and second termination trenches is allowed to float electrically.

3. The semiconductor die of Claim 1 wherein the second layer comprises a substrate and a first epitaxial layer overlying said substrate.

4. The semiconductor die of Claim 3 wherein the first layer comprises a second epitaxial layer of the first conductivity type formed on top of the first epitaxial layer.

5. The semiconductor die of Claim 1 wherein said conductive material comprises polysilicon.

6. The semiconductor die of Claim 1 wherein said dielectric layer lining each of said termination trenches comprises a thick portion at bottom of said trench.

7. The semiconductor die of Claim 1 comprising first and second contact regions of said second conductivity at said surface of first layer, said first and second contact regions being doped with a dopant of said first conductivity type to a doping concentration greater than a doping concentration of said first layer, said first contact region being located adjacent an interface between said first metal layer and said first layer, said second contact region being located adjacent an interface between said second metal layer and said first layer.

8. A semiconductor die containing an MIS device, said die comprising a first layer of a first conductivity type overlying a second layer of said first conductivity type, and a body region of a second conductivity type opposite to said first conductivity type overlying said first layer, said die further comprising:

a plurality of trenches, said trenches comprising active trenches and termination trenches, each of said trenches extending downward from a surface of said die through said body region and having a bottom located in said first layer;

a plurality of mesas located between said trenches and between one of said termination trenches and an edge of said die;

an active area comprising an MIS device, said MIS device comprising:

an active trench comprising a conductive gate material; and

a source region of said first conductivity type located adjacent said surface of said die and a sidewall of said active trench; and

a termination region comprising:

at least a first and a second termination trench, each of said termination trenches comprising a conductive material, said conductive material in each of said termination trenches being insulated from said body region and said first layer by a dielectric layer lining the sidewalls and bottom of said termination trench;

at least a first and a second metal layer above said surface of said die, said first metal layer being electrically connected to said conductive material in said first termination trench and a first portion of said body region in a first mesa between said first and second trenches, said second metal layer being electrically connected to said conductive material in said second termination trench and to a second portion of said body region in a second mesa on a side of said second termination trench opposite from said first mesa, wherein said conductive materials in said termination trenches are electrically isolated from each other and from said source region and said first layer.

9. The semiconductor die of Claim 8 wherein each of said first and second mesas comprises a heavily-doped contact region of said second conductivity type at a surface of said die, said first and second metal layers being in contact with the heavily-doped contact regions in said first and second mesas, respectively.

10. A method of forming a semiconductor die containing an MIS device comprising:

providing a semiconductor substrate;

forming an epitaxial layer of a first conductivity type on said substrate, said substrate having a net doping concentration of a second conductivity type opposite to said first conductivity type;

etching a plurality of trenches in said epitaxial layer thereby forming a plurality of mesas between said trenches and between one of said trenches and an edge of said die, said trenches extending from a surface of said epitaxial layer and having bottoms in said epitaxial layer, said trenches comprising active trenches and termination trenches, said mesas comprising active mesas

between said active trenches and termination mesas between said termination mesas between said one of said trenches and said edge of said die;

introducing a dopant of said second conductivity type through the bottoms of said active trenches and said termination trenches to form a region of said second conductivity type extending between each of said trenches and said substrate;

forming an oxide layer on the walls of said trenches;

filling said trenches with a conductive material;

implanting a dopant of said second conductivity type into said layer so as to form source regions adjacent said active trenches while preventing said dopant from entering said layer in locations adjacent said termination trenches;

forming a dielectric layer over the surface of said first layer;

masking and etching said dielectric layer so as to form openings over said source regions, said termination trenches and said termination mesas;

depositing metal over said dielectric layer and said openings;

masking and etching said metal so as to form a source metal layer extending into said openings over said source regions and a plurality of termination metal layers, said termination metal layers being electrically isolated from each other, each of said termination metal layers extending into one of said openings over said termination trenches and one of said openings over said termination mesas and electrically connecting the conductive material in one of said termination trenches and a termination mesa.

11. The method of Claim 10 comprising implanting a dopant of said first conductivity type through said openings in said dielectric layer over said termination mesas to form contact regions.

12. The method of Claim 10 wherein providing a semiconductor substrate comprises forming a second epitaxial layer of said second conductivity type on a semiconductor member of said second conductivity type.